

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R036-96. – drw	96-01-11	Michael A. Frye
B	Incorporate rev. A NOR. Update drawing to current requirements. – drw	04-03-25	Raymond Monnin

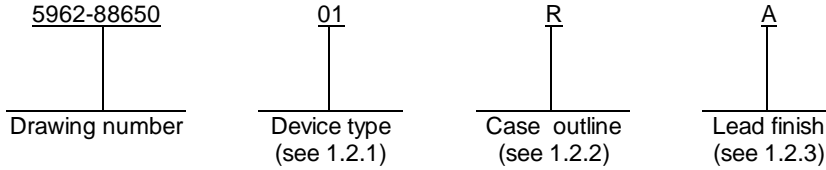
THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

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REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13						
PMIC N/A	PREPARED BY Gary Zahn	<p align="center">DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 http://www.dsc.dla.mil</p>																		
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Raymond Monnin																			
	APPROVED BY Michael A. Frye	<p align="center">MICROCIRCUIT, LINEAR, CMOS, 8-BIT, MICROPROCESSOR COMPATIBLE, A/D CONVERTER, MONOLITHIC SILICON</p>																		
	DRAWING APPROVAL DATE 89-05-30																			
	REVISION LEVEL B	<table border="1"> <tr> <td>SIZE A</td> <td>CAGE CODE 67268</td> <td>5962-88650</td> </tr> </table>	SIZE A	CAGE CODE 67268	5962-88650															
SIZE A	CAGE CODE 67268	5962-88650																		
SHEET		1 OF 13																		

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Total unadjusted error</u>
01	AD7820U	CMOS 8-bit ADC with T/H	±0.5 LSB
02	AD7820T	CMOS 8-bit ADC with T/H	±1.0 LSB

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
R	GDIP1-T20 or CDIP2-T20	20	dual-in-line
2	CQCC1-N20	20	square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage to ground (V_{DD}).....	0 V dc to +7.0 V dc
Digital input voltage	-0.3 V dc to V_{DD}
Digital output voltage.....	-0.3 V dc to V_{DD}
Positive reference voltage	V_{REF-} to V_{DD}
Negative reference voltage	0 V dc to V_{REF+}
Input voltage (V_{IN}).....	-0.3 V dc to V_{DD}
Storage temperature range.....	-65°C to +150°C
Lead temperature (soldering, 10 seconds).....	+300°C
Power dissipation (P_D)	450 mW 2/
Thermal resistance, junction-to-case (θ_{JC}):	
Cases R and 2.....	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):	
Cases R and 2.....	120°C/W
Junction temperature (T_J).....	+150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}).....	+4.75 V dc to +5.25 V dc
Positive reference voltage (V_{REF+}).....	+5.0 V dc
Negative reference voltage (V_{REF-}).....	0 V dc
Ground potential (GND).....	0 V dc
Ambient operating temperature range (T_A).....	-55°C to +125°C

1/ All voltages are with respect to ground.
 2/ Derate above $T_A = +75^\circ\text{C}$ at 6.0 mW/°C.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-88650
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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution	RES	This is the minimum resolution for which no missing codes are guaranteed	1, 2, 3	All	8.0		LSB
Total unadjusted error	TUE	<u>3/</u>	1	01		±1	LSB
			2, 3, 12			±0.5	
			1, 2, 3	02		±1	
Analog input leakage current	I _{IN}		1, 2, 3	All		±3.0	μA
Analog input capacitance	C _{IA}	See 4.3.1c, T _A = +25°C	4	All		60	pF
Reference input resistance	R _{IN}		1, 2, 3	All	1.0	4.0	kΩ
Digital input high level voltage	V _{IH}	$\overline{\text{CS}}$, $\overline{\text{WR}}$ and $\overline{\text{RD}}$ inputs (pin 7)	1, 2, 3	All	2.4		V
		Mode input			3.5		
Digital input low level voltage	V _{IL}	$\overline{\text{CS}}$, $\overline{\text{WR}}$ and $\overline{\text{RD}}$ inputs (pin 7)	1, 2, 3	All		0.8	V
		Mode input				1.5	
Digital input high current	I _{IH}	$\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs	1, 2, 3	All		±1.0	μA
		$\overline{\text{WR}}$ input				±3.0	
		Mode input (pin 7)				±200	
Digital input low current	I _{IL}	$\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$ and mode inputs (pin 7)	1, 2, 3	All		-1.0	μA
Digital input capacitance	C _{ID}	$\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$ and mode inputs, See 4.3.1c, T _A = +25°C	4	All		8.0	pF
Digital output high level voltage	V _{OH}	DB ₀ – DB ₇ , $\overline{\text{OFL}}$, and $\overline{\text{INT}}$ outputs, I _{SOURCE} = 360 μA	1, 2, 3	All	4.0		V
Digital output low level voltage	V _{OL}	DB ₀ – DB ₇ , $\overline{\text{OFL}}$, and $\overline{\text{INT}}$ outputs, I _{SINK} = 1.6 mA	1, 2, 3	All		0.4	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions <u>1/2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Floating state leakage current	I _{OUT}	DB ₀ – DB ₇	1, 2, 3	All		±3.0	μA
Digital output capacitance	C _{OUT}	See 4.3.1c, T _A = +25°C	4	All		8.0	pF
Supply current from V _{DD}	I _{DD}	$\overline{CS} = \overline{RD} = 0\text{ V}$	1, 2, 3	All		20.0	mA
Power supply sensitivity	PSS	V _{DD} = 5 V ±5%	1, 2, 3	All		±.25	LSB
\overline{CS} to $\overline{RD}/\overline{WR}$ setup time	t _{css}	<u>6/</u> , <u>7/</u>	9, 10, 11	All	0		ns
\overline{CS} to $\overline{RD}/\overline{WR}$ hold time	t _{CSH}	<u>6/</u> , <u>7/</u>	9, 10, 11	All	0		ns
\overline{CS} to RDY delay	t _{RDY}	C _L = 50 pF, Pull-up resistor = 2.0 kΩ <u>6/</u> , <u>7/</u>	9 10, 11	All		70 100	ns
Conversion time (RD mode)	t _{CRD}	See figure 3. <u>7/</u>	9 10, 11	All		1.6 2.5	μs
Data access time (RD mode)	t _{ACCO}	<u>4/</u> , <u>7/</u>	9 10, 11	All		1.62 2.55	μs
\overline{RD} to \overline{INT} delay (RD mode)	t _{INTH}	C _L = 50 pF <u>7/</u>	9 10, 11	All		175 225	ns
Data hold time	t _{DH}	<u>5/</u> , <u>6/</u> , <u>7/</u>	9 10, 11	All		60 100	ns
Delay time between conversion	t _P	<u>6/</u> , <u>7/</u>	9 10, 11	All	500 600		ns
Write pulse width	t _{WR}	<u>6/</u>	9, 10, 11	All	0.6	50	μs
Delay time between \overline{WR} and \overline{RD} pulses	t _{RD}	<u>6/</u>	9 10, 11	All	600 700		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions <u>1/ 2/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data access time ($\overline{\text{WR}}$ / $\overline{\text{RD}}$ mode)	t _{ACC1}	<u>4/</u> , <u>6/</u>	9	All		160	ns
			10, 11			250	
$\overline{\text{RD}}$ to $\overline{\text{INT}}$ delay	t _{R1}	<u>6/</u>	9	All		140	ns
			10, 11			225	
$\overline{\text{WR}}$ to $\overline{\text{INT}}$ delay	t _{INTL}	C _L = 50 pF <u>6/</u>	9	All		1.0	μs
			10, 11			1.7	
Data access time ($\overline{\text{WR}}$ / $\overline{\text{RD}}$ mode)	t _{ACC2}	<u>4/</u> , <u>6/</u>	9	All		70	ns
			10, 11			110	
$\overline{\text{WR}}$ to $\overline{\text{INT}}$ delay (Stand alone operation)	t _{IHWR}	C _L = 50 pF <u>6/</u>	9	All		100	ns
			10, 11			150	
Data access time after $\overline{\text{INT}}$ (Stand alone operation)	t _{ID}	<u>6/</u>	9	All		50	ns
			10, 11			75	

1/ V_{DD} = +5.0 V; V_{REF(+)} = +5.0 V; V_{REF(-)} = GND = 0 V unless other wise specified. Specifications apply for $\overline{\text{RD}}$ mode (pin 7 = 0 V).

2/ All input control signals are specified with t_r = t_f = 20 ns (10 percent to 90 percent of +5.0 V) and timed from a voltage level of 1.6 V.

3/ Includes gain error, offset error and linearity error.

4/ Measured with load circuits of figure 2 and defined as the time required for an output to cross 0.8 V to 2.4 V.

5/ Defined as the time required for the data lines to change 0.5 V when loaded with the circuits of figure 2 and is measured only for the initial test and after process or design changes which may affect t_{DH}.

6/ Refer to timing diagrams of figure 3. These parameters, if not tested, shall be guaranteed to the limits specified in table I.

7/ Refer to timing diagram of figure 3 ($\overline{\text{RD}}$ mode). These parameters are tested to subgroup 9 under group A test requirements.

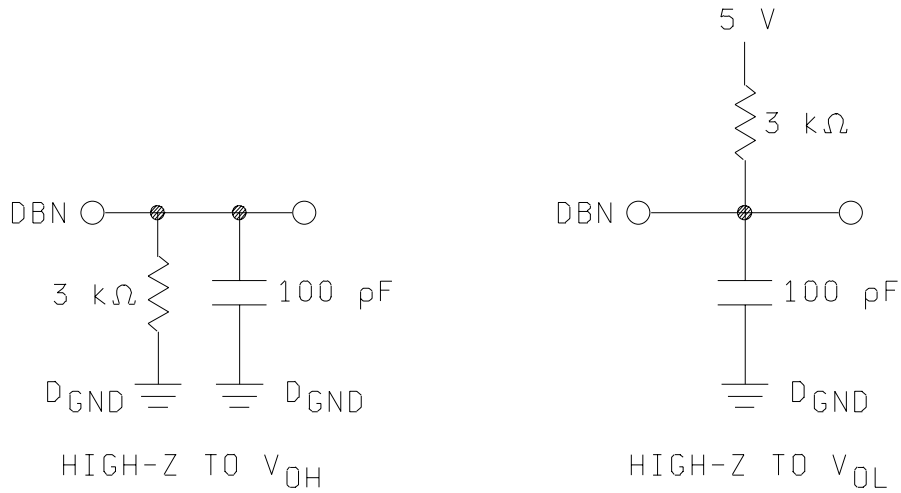
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-88650
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Device types	All
Case outlines	R and 2
Terminal number	Terminal symbol
1	V _{IN}
2	DB0(LSB)
3	DB1
4	DB2
5	DB3
6	$\overline{\text{WR}}/\text{RDY}$
7	MODE
8	$\overline{\text{RD}}$
9	$\overline{\text{INT}}$
10	GND
11	V _{REF-}
12	V _{REF+}
13	CS
14	DB4
15	DB5
16	DB6
17	DB7(MSB)
18	$\overline{\text{OPL}}$
19	NC
20	V _{DD}

FIGURE 1. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-88650
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LOAD CIRCUITS FOR DATA ACCESS TIME



LOAD CIRCUITS FOR DATA HOLD TIME

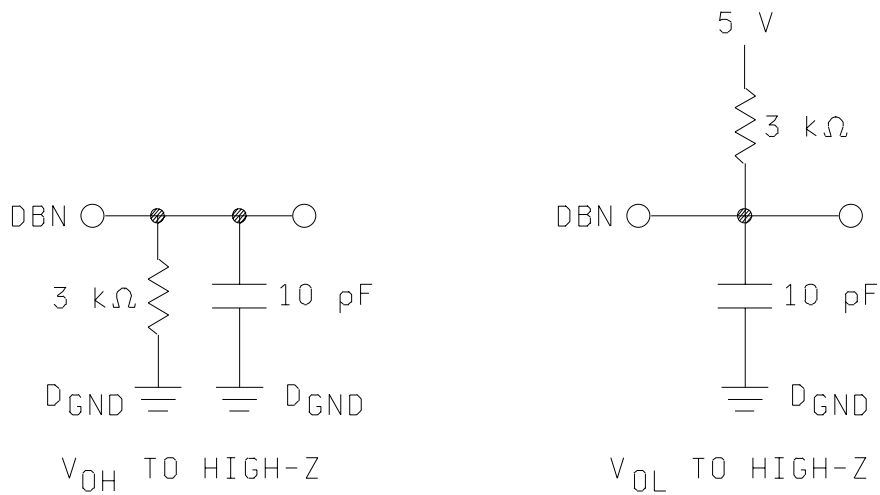


FIGURE 2. Output load circuits.

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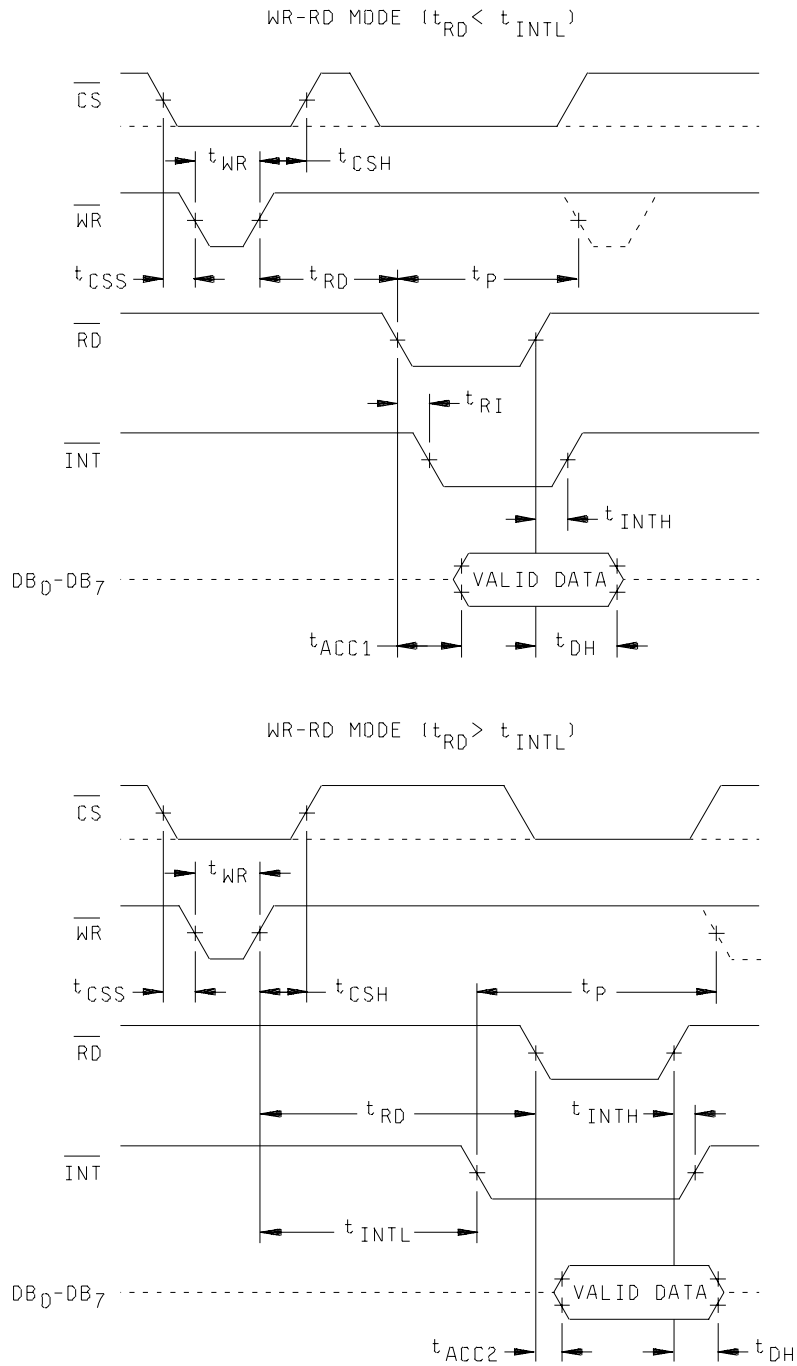


FIGURE 3. Mode timing waveforms.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-88650
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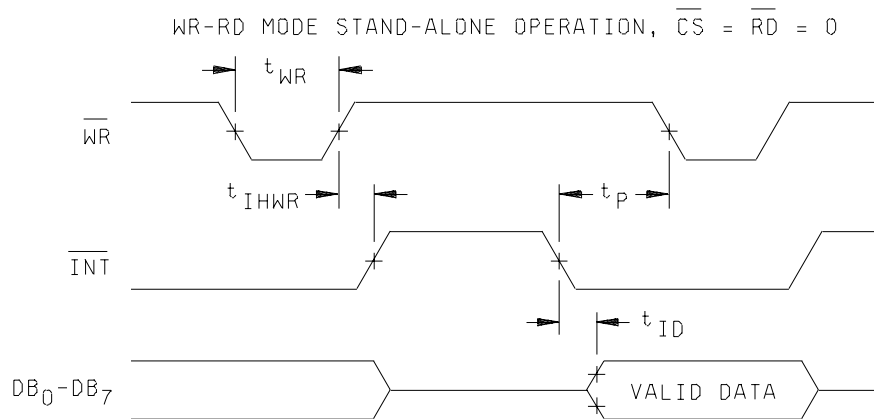
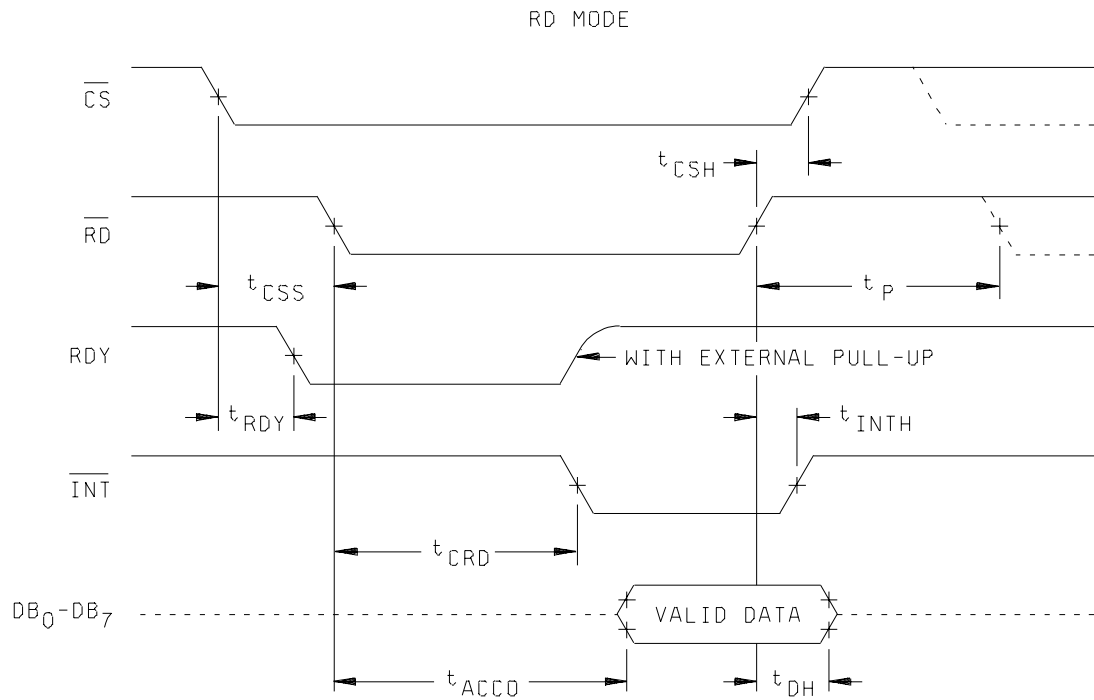


FIGURE 3. Mode timing waveforms - continued.

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MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

5962-88650

REVISION LEVEL
B

SHEET
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3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 12
Group A test requirements (method 5005)	1, 2, 3, 4, 9, 10**, 11**, 12
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.

** Subgroups 10 and 11 if not tested, are guaranteed to the limits specified in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_{IA} , C_{ID} , and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.
- d. Subgroup 12 test is used for grading and part selection at $T_A = +25^\circ\text{C}$ and is not included in PDA calculations.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 04-03-25

Approved sources of supply for SMD 5962-88650 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-88650012A	24355	AD7820UE/883B
5962-88650012C	1ES66	MX7820UE/883B
5962-8865001RA	24355	AD7820UQ/883B
	1ES66	MX7820UQ/883B
5962-88650022A	24355	AD7820TE/883B
5962-88650022C	1ES66	MX7820TE/883B
5962-8865002RA	24355	AD7820TQ/883B
	1ES66	MX78020TQ/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

Vendor name and address

24355

Analog Devices
Rt 1 Industrial Park
PO Box 9106
Norwood, MA 02062

Point of contact:
Raheen Business Park
Limerick, Ireland

1ES66

Maxim Integrated Products
120 San Gabriel Dr
Sunnyvale, CA 94086-5125

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